

On Wafer Noise Measurement Using Bipolar Transistor RF Test Structures

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Abstract:- We present here a technique for on wafer noise we measurements using bipolar R.F. cell structures. Measurements were taken using both single and multiple device placements on a variety of technologies. At mid band, identification of individual noise sources within the device allows us to extract a base spreading resistance parameter. This noise extracted value for r_b is compared to data from 'S' parameter measurement and our noise measurements are tested against simulated mid-band noise profiles.

INTRODUCTION

Noise Measurement Equipment

All mid band noise figure measurements were taken using an HP8970B (unexpanded) noise figure meter (10MHz to 1.6 GHz) with

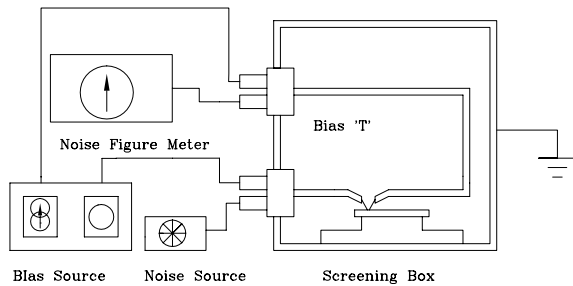


Fig (1.0) The Noise Measurement System

a measurement bandwidth of 4MHz. For measurement frequencies in excess of 1.6 GHz a Maury Microwave extender box was used to produce an I.F. of 30 MHz from measurement frequencies up to 18 GHz, these being generated by an external local oscillator (HP8341B Frequency Sweeper). Excess noise was generated from an HP346B noise source which produces 15 dB of white noise up to 18 GHz. This in essence is just an avalanche diode matched to a 50 Ω environment. R.F. footprint transistor structures were probed on wafer using Cascade co-planar tungsten probes housed in a purpose-built screened enclosure. Biasing was accomplished by means of a standard HP4145 parametric analyser and a pair of HP11612A bias networks with a frequency response (3dB to 3dB) of 45MHz to 26.5 GHz. Care was taken to ensure that both airborne R.F. and line noise were excluded. A symbolic representation of the measurement system is shown in Fig(1.0).

Noise Figures of Amplifier Systems

The noise figure of an amplifier system provides a convenient figure of merit for noise performance. It is simply the ratio of the signal to noise figures taken at the input and output of the system. Figures quoted in this report are for N_f (dB) as:

$$N_f(\text{dB}) = 10 \log \left(\frac{S_n(o)}{S_n(i)} \right) \quad (1)$$

Another way in which N_f is defined is in terms of a noiseless amplifier having a 'noisy' source resistance R_s at the input. In this case the Johnson (thermal) noise of the source resistance is taken as the input signal and the noise figure is defined as:

$$N_f(\text{dB}) = 10 \log \left(1 + \frac{V_n^2}{4kTR_s} \right) \quad (2)$$

Where V_n^2 is the mean square noise voltage contribution per hertz with a cold (noiseless) source resistance of R_s connected at the amplifier's input. Although noise figures provide a convenient measure of noise performance it is easy to be mis-lead as there is a heavy dependence upon the source resistance R_s . Noise figures are often quoted by semi-conductor manufacturers, but these may be minimum figures obtained at optimum values of source resistance and at the most favourable operating point for the device. It is often better to think in terms of the signal to noise ratio of the system which can be calculated from N_f . Assuming an R.M.S. signal amplitude of V_s we calculate:

$$S_n = 10 \log \left(\frac{V_s^2}{4kTR_s} \right) - N_f(\text{dB}) \Big|_{R_s} \quad (3)$$

NOISE SOURCES IN BIPOLAR TRANSISTORS

Noise generation in bipolar transistors can be divided into five broad areas; we consider each here briefly and without derivation.

Thermal (Johnson) Noise

The thermal noise component is due to the random thermal excitation of carriers. Thus any ohmic resistive elements will produce thermal or Johnson noise. The magnitude of this noise source is dependent on the value of the resistor and the absolute temperature only. 'Quality' factors are not significant as the noise current generated is due to thermal fluctuations only. The mean square Johnson noise voltage developed across the terminals of a resistor is given by:

$$\overline{V_n^2} = 4kTR \cdot \Delta f \quad (4)$$

where N_f is the measurement bandwidth. Johnson noise is 'white' in nature and of interest across the whole of the noise spectrum.

Shot Noise

Shot noise reflects the discrete nature of the charge carriers and the

resultant fluctuation in current density emitted from junctions and surfaces. The mean square fluctuation of the number of carriers is related only to the average number of carriers emitted and is given by :-

$$\overline{In^2} = qI \cdot \Delta f \quad (5)$$

Shot noise is again white in nature and of interest across the whole noise spectrum.

Flicker (1/f) Noise

Flicker noise or '1/f' noise as it is sometimes called is probably the least well understood noise mechanism in bipolar transistors and there are many factors which may contribute to the overall flicker noise performance of a device. Flicker noise is generally held to be defect dependent. Recombination centres within space charge regions and slow interfacial oxide traps are thought to be the dominant features but lattice straining and grain boundary effects (in polysilicon emitters) may also contribute. Recent work by Jones et al [1] suggests that the predominant contribution to 1/f noise in bipolar transistors is due to generation/recombination currents at the oxide-EB depletion region interface. Thus

$$\overline{If^2} = K \frac{I_{B0}}{f^\lambda} \cdot \Delta f \quad (6)$$

with $\lambda \approx 1$. I_{B0} represents some average value of the non-ideal base current at the relevant bias point. It is obvious from the above that flicker noise exhibits a 1/f spectrum. The frequency at which mid band noise contributions become comparable to that from 1/f sources (1/f corner frequency) should for a good device be as low as possible.

A SIMPLIFIED HYBRID- π MODEL INCLUDING NOISE SOURCES

We do not present a full derivation of noise figure for a bipolar transistor here. The reader is referred to the literature, specifically Nielson for an initial model [2] and Hawkins [3] for a discussion of its limitations. For a full model we must consider the effects of device transit times and of the frequency dependent contribution to the emitter resistance. It is important to identify the dominant time constants as earlier theories assume that the transistor is dominated only by the base transit time. Hawkins has allowed for this and added terms to correct for the existence of multiple time constants. If, however, we choose our measurement area and operating point carefully the situation is somewhat simpler and many terms may be discarded as they are now of little significance. Fig(2.0) shows a simplified hybrid- π equivalent circuit with the major noise sources inserted. This model contains no frequency dependent resistances and does not include any junction capacitances or Miller capacitances. Although in our case the source resistance is fixed at 50Ω in our equivalent circuit and its subsequent treatment we include it as either the admittance G_s or the resistance R_s . Noise sources are included as either noise currents or equivalent noise voltages with the appropriate noiseless resistance or admittance. R_i represents the dynamic component to the base resistance whilst we represent the dynamic (slope) resistance value of the emitter resistance as r_e .

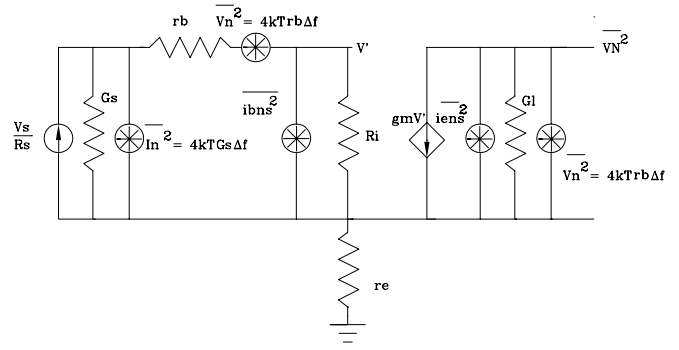


Fig (2.0) Noise Model Of Bipolar Transistor At Midband

We may then use this circuit to sum the noise contributions from each source, at the collector to produce a noise figure for the transistor. It is worth remembering at this point (especially for those unfamiliar with noise analysis) that it is the R.M.S. values of the individual noise sources that are added, assuming them to be un-correlated. We also assume here that we are well away from the flicker noise corner frequency and so any 1/f type contributions are negligible. Following through the analysis of the circuit given in Fig(2.0) results in an expression for the noise figure of the transistor (assuming r_b as a particular value of R_{bb}) as :-

$$N_f(\text{dB}) = 10 \log \left[1 + \frac{r_b}{R_s} + \frac{(r_b + R_s)^2 q I_e}{2kT R_s \beta} + \frac{q I_e}{2kT R_s \beta} \left(\frac{r_b + R_s + \beta r_e}{\beta} \right)^2 \right] \quad (7)$$

This is often further simplified by assuming a constant b for the operating region of interest as this reduces the number of terms to be considered when solving the quadratic for r_b . We choose however to retain those terms in b to account for gain roll-off at high values of I_e . We can then solve for r_b in the usual fashion, the standard quadratic

$$a \cdot r_b^2 + b \cdot r_b + c = 0 \quad (8)$$

having coefficients

$$a = 1 + \frac{1}{\beta^2}$$

$$b = 2 \left(b r_e + R_s + \frac{R_s}{\beta^2} + \frac{r_e}{\beta} \right)$$

$$c = R_s^2 + r_e^2 + \left(\frac{R_s}{\beta} \right)^2 + \frac{2 r_e R_s}{\beta} - 2 \beta r_e R_s (10^{N_f(\text{dB})/10} - 1)$$

Thus if we choose values of I_e and plot against R_s we describe constant contours of N_f as shown in Fig(2.1). Assuming a constant known

value of R_s (a $50\ \Omega$ noise source in this case), we would expect to see a 'U' shaped response for a plot of N_f against I_e (see Fig(2.2)). This can be understood in terms of the dominant noise source contributions at any particular bias point. At low emitter currents we have a high dynamic emitter resistance r_e , which causes a large shot noise related component, dominating the noise figure.

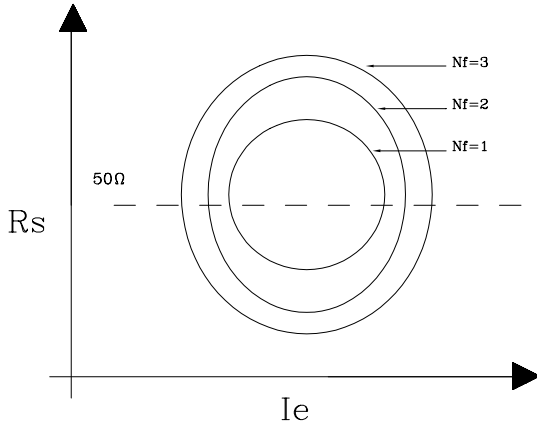


Fig (2.1) Contours of Constant N_f

As we move to higher emitter currents this contribution falls off and we reach a noise minimum. Here the noise figure of the transistor is dominated by Johnson noise developed across the ohmic base spreading resistance. It is to be expected that the larger the transistor, the lower this minimum noise figure will be. At higher emitter currents the base shot noise becomes large enough to dominate and we move away from the thermal noise minimum.

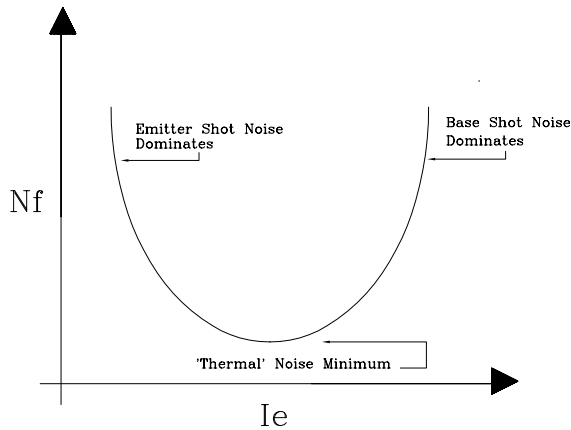


Fig (2.2) Noise Profile For Constant R_s

Of course other mechanisms may be present which contribute to the overall noise figure and they will contribute excess noise over and above that predicted by Eqn (7). In the derivation of Eqn(7) our simplification of the 'real' transistor impinges directly on our choice of measurement frequency and lower bias point for noise measurement. For our assumptions to hold we must satisfy the following inequality:-

$$\frac{I_{co}}{I_e} \ll \left(\frac{f}{f_\alpha} \right)^2 \ll \frac{1}{\beta}$$

The parameter f_α is the cut-off frequency for the transistor in common base mode and is generally related to the common emitter cut off frequency by a factor close to unity. This is a sufficiently close approximation for us to be able to determine our frequency 'window' for mid band noise measurement. As a spot measurement frequency we choose to operate at around 200 MHz which satisfies all criteria for mid band noise measurement as modelled by the preceding equations.

TEST STRUCTURES

Initially no special structures were available and so measurements were taken using the R.F. test structures already present on the test wafers. These consist of either single or multiple placements of transistors (parallel) within a ground-signal-ground R.F. pad footprint. Although both common emitter and common base layouts were available we chose to consider the common emitter configuration only. Ideally single transistor instances should be used for noise measurements where possible as this avoids the problem of considering which (if any) of the noise sources in a parallel structure should be considered to be correlated. Unfortunately for some of the device geometries only multiple placements were available. Although this complicates the noise analysis it does allow us to make some interesting inferences on paralleled transistor structures in general. The excess noise of the complete measurement system was calibrated out using an R.F. through structure which ensured that all non-DUT noise contributions (connectors, probe contact resistance etc.) were nulled. More recent measurements (process HG) have involved the use of dedicated 'noise' R.F. cells containing an integral 'through' structure. Probe pressure and ageing are known to contribute greatly to measurement error and the availability of a local calibration site adds to repeatability

EXPERIMENTAL TECHNIQUE

Great care must be taken with any noise measurement, as by the very nature of the data being sought environmental conditions can effect the measurement considerably. Ideally such measurements should be made under fully E.M. screened conditions in a noise isolation room. Unfortunately, due to logistical problems this was not possible and other screening options had to be considered. A first attempt was made at taking measurements on a completely unshielded probe station. This proved highly impractical as even when good calibrations were obtained the system was too unstable for any useful measurements to be made. It was then decided to commission the fabrication of an aluminium prober enclosure into which the prober could be placed. This yielded an immediate and profound increase in system stability. All possible electrical noise sources were excluded from the enclosure, and care was taken to ensure that the box was well grounded. Multiple groundings are to be avoided in noise measurements and the system ground was generally chosen to be the D.C. bias instrument's shield terminal, the guard of which was left at a floating potential. Excess system noise was calibrated out using an R.F. on wafer through structure close to the measurement site. Calibrations made at the measurement frequency were accepted if the residual system noise after correction was better than ± 0.1 dB. Noise measurements were accepted if on returning to the calibration site, the system residual noise was still less than our arbitrary ± 0.1 dB limit. For R_{bb} extraction this imposes an absolute system accuracy of $\pm 3\ \Omega$. Measurements were also rejected if the insertion gain of the device fell to less than -3 dB.

Parallel Test Structures

Although ideally single instances of devices should be used for noise characterization, many devices were only represented as multiple parallel placements in an R.F. footprint cell. We must therefore consider carefully the implications of having individual transistors contributing to what is a composite noise figure for the total structure. Consider the noise profile shown in Fig(2.2). At low emitter current densities the noise figure is dominated by shot noise being amplified across a large dynamic emitter resistance r_e . The shot noise contribution from any element of a parallel transistor array depends on the quantization of current flow at that particular junction at that particular instant. These then cannot be correlated. This leads to the fact that for any number of parallel devices, the current densities in each individual device are unimportant as long as they are equal. The noise generated by the structure in this region is a function of the total emitter current and device gain only and not related to current density. Thus the value for r_e placed in Eqn(7) should be that given by the expression:

$$r_e = \frac{kT}{qI_t}$$

Where I_t is the total emitter current flowing in the structure. As we pass through the noise minimum of the structure we again encounter a shot noise dominated region, as the major contribution to the overall noise figure becomes due to current noise within the base of each individual transistor. Again we should see the noise figures for parallel structures of any number converge as the noise contribution is dependent on the absolute current flowing in the test structure and its current gain. As the noise minimum is approached however, the major contribution becomes that of a thermal noise current flowing through a compound paralleled value of R_{bb} . This same noise current flows through all devices, so we should expect these contributions to be correlated, that is to say that any value of R_{bb} extracted from Eqn(7) will be that for a parallel structure. Although this contribution has terms in β they are second order and the minimum noise figure for the device is largely independent of device gain.

MEASUREMENT RESULTS

Measurements were taken on three device technologies. Process WQ a well established junction isolated technology, process HE an advanced self aligned technology with trench isolation and process HG a 'cutting edge' bipolar process similar to process HE but with reduced dimensions. The dimensions and structural details of each device are given in appendix A at the foot of the paper.

The following RF cell structures were selected for test on process WQ:

- i) Transistor xa1d25 single placement
- ii) Transistor xa1d25 five parallel
- iii) Transistor xa1d25 ten parallel

and for process HE we chose some large hopefully low noise devices as

- i) Transistor wb15 single placement
- ii) Transistor wf15 single placement
- iii) Transistor ww15 single placement

The devices for HG were also chosen as the largest standard layouts available, those being

- i) Transistor yaa4 single placement
- ii) Transistor yf4 single placement
- iii) Transistor yd3 single placement

Single and parallel Transistor Structures

The first device to be investigated was the HE wb15 transistor. Noise measurements were taken with the transistor biased in the active region with V_{ce} at 2v and base currents being driven at between 1 μ A and 1mA. Fig(3.0) shows the recorded noise figures at 200 MHz, the form of the curve being as we expect from our earlier discussion. We

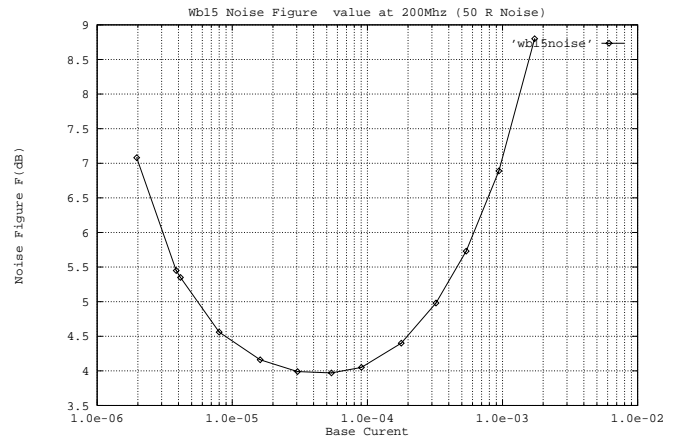
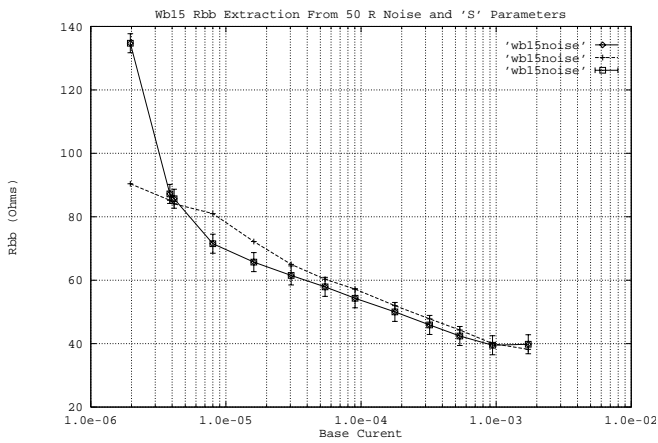


Fig (3.0) 50 Ω Noise Profile Of wb15 Device

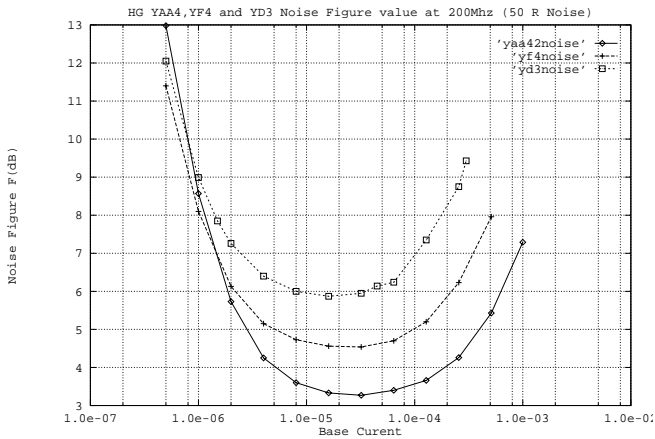
note that the minimum noise figure for this device is just below 4 dB and that it occurs at a bias point corresponding to a base current drive of around 500 μ A. Using Eqn(7) it is possible to isolate the contribution to the noise figure due solely to Johnson noise across R_{bb} . Fig(3.1) shows the extracted value of R_{bb} plotted against I_b . The same device was then characterised using 'S' parameter measurements and the R_{bb} values re-extracted. These are plotted on the same axis as the noise derived results in Fig(3.1). Error bars have been placed upon the noise extraction results to indicate the limits of the ± 0.1 dB system resolution. It can be seen that over most of the area of interest there is very good agreement between the R_{bb} values extracted using both techniques. This leads to two important conclusions, firstly we may now be re-assured that R_{bb} values obtained by reflection data do in fact represent some 'real' ohmic resistance within the device, ie the 'S' parameter model is correct. Secondly we note that the device does not produce any 'excess' noise over and above those due to the contributions we considered above. It can be seen that the noise extracted value for R_{bb} becomes increasingly more inaccurate as we tend to lower base currents, and indeed for base currents where we would expect to see an R_{bb} maximum plateau the noise extracted figure tends to infinity. This is to be expected as at low current densities our simple hybrid-pi noise model breaks down and a more complex model is required, one which includes frequency dependent contributions to r_e as well as various time constants and diffusion capacitances [3]. We next consider the noise performance of the HG yaa4, yf4 and yd3 devices which we plot against the same axes in Fig(3.2). The conver-

gent ‘current driven’ shoulders of each curve can clearly be observed, as well as a broad noise minimum.



Fig(3.1) Rbb Against I_b Extracted From Noise and 'S' Parameter Data

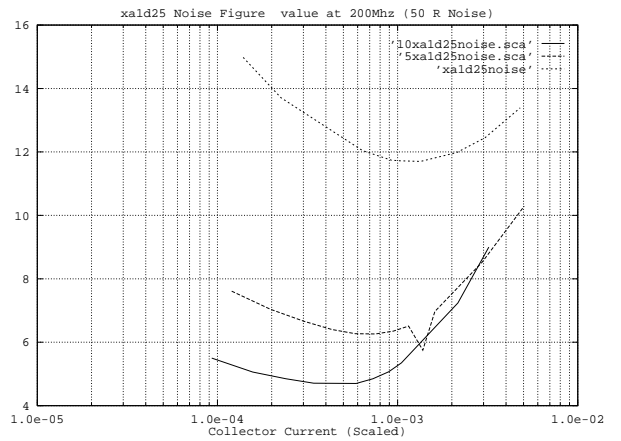
As we would expect, the larger the device, the lower the minimum noise figure. The results for both 'S' parameter and noise extraction for our parallel structures are plotted on Fig(3.4). Again we see that at low emitter currents the model breaks down and there is a rapid divergence between noise and 'S' parameter measurements. It is interesting to note however that where our model is claimed to be valid we see that there is still very good agreement between both sets of extractions.



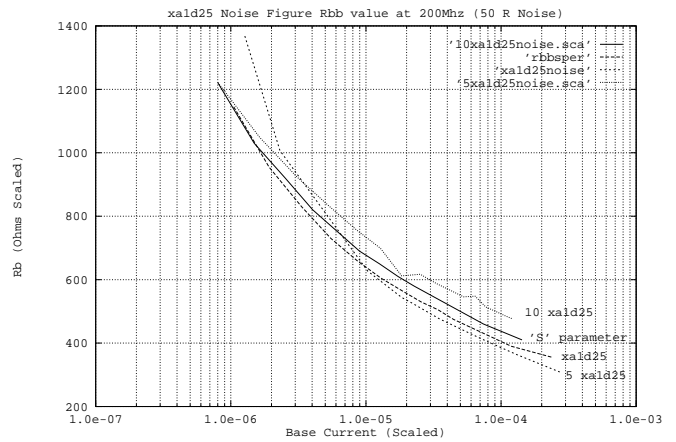
Fig(3.2) Noise Profiles For Progressively Larger Transistor Geometries

NOISE SIMULATION

As a final check on the validity of our extractions of parameters from noise modelling and other characterization techniques we would do well to compare our measured noise data with that obtained from simulation. By this technique we ensure that our assumptions about the device are valid (our simplified noise model) and that our devices are not excessively noisy. We present here data for the HG yf4 device from simulations using the H.P. EESOF tools. Fig(4.0) shows the simulation circuit including bias networks, sources and implicit 50 Ohm terminations. This test ‘harness’ is then placed as an element, along with D.C. bias sources into a EESOF Linear Bench analysis for noise simulation.

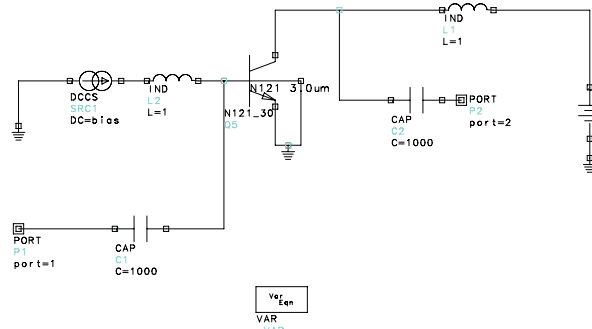


Fig(3.3) Noise Profiles For Parallel Transistor Structures



Fig(3.4) Extracted Rbb Profiles For Parallel Structures

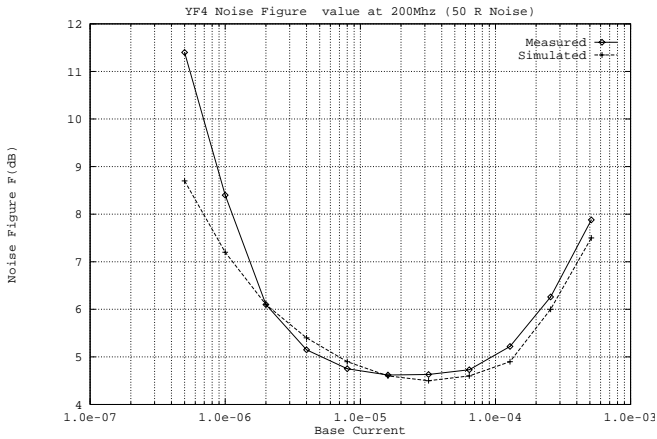
Fig(4.1) shows a comparison between measured noise figure and simulated, over a bias range of 0.4uA to 400uA. The important features being the coincident noise minima and for currents greater than 2uA a maximum discrepancy between the two curves of around 0.5 dB.



Fig(4.0) The Noise Simulation Circuit

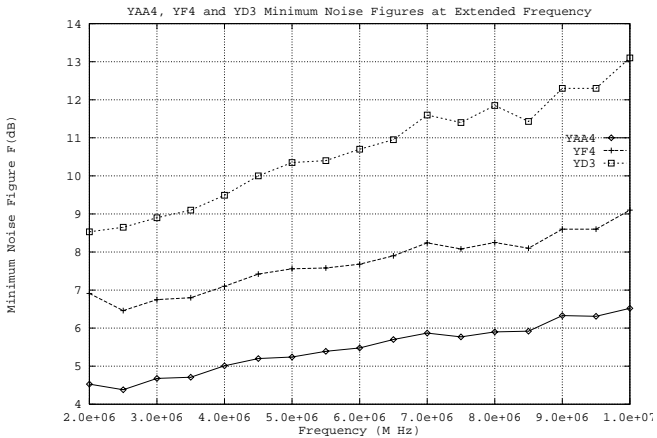
NOISE MEASUREMENTS AT EXTENDED FREQUENCIES

As we move away from the mid-band region towards higher measurement frequencies the noise profile once more begins to exhibit some frequency dependence. This has been explained in terms of a frequency related component in the shot noise [4]. We would expect to see a monotonic increase in N_f with frequency.



Fig(4.1) Simulated Noise Profile Against Measured Data.

Noise measurements were made up to 1.6 GHz using the HP 8970B in unexpanded mode and from 1.6 GHz to 10 GHz using a Maury Microwave noise extender. In this mode a local oscillator is required to supply the sampling frequency, the output from the noise extender being set to an I.F. of 30 MHz.



Fig(5.0) 50 Ohm Minimum Noise Figure Measurements at Extended Frequency

Minimum noise figures for the yaa4, yf4 and yd3 were recorded at frequencies of up to 10 GHz. In practice it was found that calibrations at higher frequency were more prone to drift and were also more sensitive to variations in probing technique (probe over-travel for example). It is important to ensure that the chosen measurement frequency is well away from either 3dB shoulder of the noise extender. In practice this meant that a more sensible range of measurement was found to be from 2.0 GHz upwards. Below this limit system losses quickly

negated the validity of any measurements. The minimum noise figures recorded for each structure are plotted against measurement frequency in Fig (5.0). The general trend is as we expected although the difficulty of the measurement is evident in the somewhat excursive profiles.

CONCLUSIONS

We have presented here an alternate route to the extraction of the base spreading resistance R_{bb} of a bipolar transistor. Results compare favourably with 'S' parameter measurement and indeed the noise technique appears to be superior when applied to large structures with low values of R_{bb} . As an integral part of the analysis we have identified individual noise sources within the device and the success of the R_{bb} extraction indicates that our model is well founded. It is interesting to note that the good agreement between 'S' parameter derived R_{bb} profiles and those obtained through noise measurements suggests that the large HE and HG devices are not excessively noisy in the mid band. High frequency measurements although not fitted to a model give results which are at least qualitatively correct and understandable. We have shown that on wafer noise characterization is possible over extended frequency ranges up to 10 GHz and beyond. Finally we have closed the measurement loop and tested our parametric extraction by comparing measured noise data against extracted.

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APPENDIX A DEVICE DIMENSIONS AND STRUCTURES

Process WQ

xa1d25 Single base single emitter (0.75 x 1.25)

Process HE

wb15 Double basesingle emitter (1.0 μ m x 15 μ m)

wf15 Triple base quad emitter (1.0 μ m x 15 μ m)

ww15 Ten base Eleven emitter (1.0 μ m x 15 μ m)

Process HG

yaa4 13 base 12 emitter (0.6 μ m x 4 μ m)

yf4 Quad base 3 emitter (0.6 μ m x 4 μ m)

yd3 Triple base double emitter (0.6 μ m x 3 μ m)

