Automated Extraction of Matching Parameters for Bipolar Transistor Technologies

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Notation

A_J, area of base emitter junction.

n_{op}, free electron concentration in quasi-neutral 'p' type material.

p_o, free hole concentration in quasi-neutral 'p' type material.

WB, width of quasi-neutral base region.

μ_e, electron mobility

x, distance.

Abstract-- We present here a technique for automatically producing statistical data for bias and resistor mis-match on bipolar transistor technologies by use of a nulled differential amplifier. The method has been developed to enable automatic wafer probe and the generation of distributions and wafer maps. The data is analysed using software from the SAS Institute and the method allows extraction of both resistor and V_{BE} mis-match from a single circuit.

Introduction

Traditionally, measurement of component matching parameters has been at best a difficult process. We would typically expect to see V_{BE} mis-matches of hundreds of microvolts against quiescent operating points of several hundred millivolts. Bridging techniques allow the quiescent voltages to be 'backed' off and reasonably accurate measurements can be taken. This approach is time consuming and does not lend itself well to automated measurement however. The use of a differential amplifier allows us to take advantage of the stage gain of the circuit and places our measurement 'envelope' in the mV range without the need to compensate for large offsets and small measurement signals [1] [2] [3][4].

The response curve for V_{BE} mis-match against emitter current generally resembles a steep sided 'U' shaped valley. At very low emitter currents localised differences in electro-chemical potential at the active emitter surface will prove significant causing great variance between devices. Similarly at high injection levels resistive losses within the extrinsic regions of the device will manifest de-biasing of the emitter base junction and large mis-matches between devices. Between these two extremes mis-match tends to be flat over several orders of magnitude (most of the active operating region of the transistor). In this regime mis-match is thought to be predominantly a function of differences in true electrical emitter width and as such subject to process variability.

A Mis-matched Long-Tail Pair

Consider the circuit of Fig(1), consisting of a long tail pair with equal load resistors and a current source sinking the total tail current . Let there be a offset between the devices of ΔV_{BE} . We may now define the collector currents flowing in each arm, Ic_1 and Ic_2 as:

$$Ic_1 = D \exp\left[\frac{qV_{BE}}{kT} + \frac{q\Delta V_{BE}}{kT}\right] \tag{1}$$

$$Ic_2 = D \exp\left[\frac{qV_{BE}}{kT} - \frac{q\Delta V_{BE}}{kT}\right] \tag{2}$$

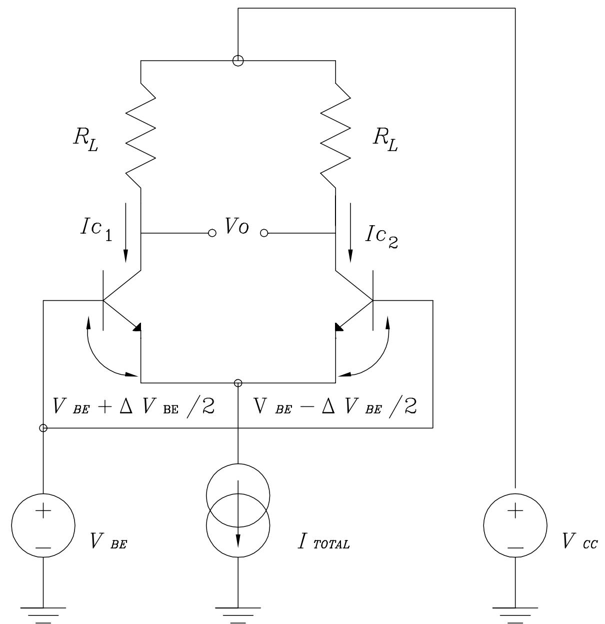


Fig (1) A Long Tailed Pair With Mis-matched Transistors

where all symbols have their normal meaning and the pseudo constant D is defined as:

$$\mathrm{D} = \mathrm{A_J} \frac{\mu_e \mathrm{kT} p_0(0).n_{0p}}{\int_0^{WB} p_0(x)\,\mathrm{dx}} \tag{3}$$

We now define an output voltage for the amplifier stage, *Vo* where $Vo = R_L\,(Ic_1 + Ic_2)$ and note that the total tail current which we call I_{TOTAL} is given by the summation of (1) and (2). Thus *Vo* is given as function of the total current, load resistance and V_{BE} mis-match as:

$$Vo = \mathrm{D}R_L \left[\begin{array}{c} \left(\exp\frac{\mathrm{q}V_{BE}}{\mathrm{kT}} \times \exp\frac{\mathrm{q}\Delta V_{BE}}{2\mathrm{kT}} \right) \\ - \\ \left(\exp\frac{\mathrm{q}V_{BE}}{\mathrm{kT}} \times \exp\frac{-\mathrm{q}\Delta V_{BE}}{2\mathrm{kT}} \right) \end{array} \right] \tag{4}$$

or,

$$Vo = I_{TOTAL} R_L \left[\frac{\exp\frac{\mathrm{q}\Delta V_{BE}}{2\mathrm{kT}} - \exp\frac{-\mathrm{q}\Delta V_{BE}}{2\mathrm{kT}}}{\exp\frac{\mathrm{q}\Delta V_{BE}}{2\mathrm{kT}} + \exp\frac{-\mathrm{q}\Delta V_{BE}}{2\mathrm{kT}}} \right] \tag{5}$$

which we recognise as the trigonometric function tanh, thus:-

$$Vo = I_{TOTAL} R_L \tanh\left(\frac{\mathrm{q}\Delta V_{BE}}{2\mathrm{kT}} \right) \tag{6}$$

RESISTOR MIS-MATCH

In practice however the load resistors in each arm of the differential pair will not be perfectly matched so we define a nominal resistor value R_{NOM} and an error term ΔR (see fig (2))such that:-

$$R_{NOM} = \frac{(R_1 + R_2)}{2} \tag{7}$$

$$\Delta R = \frac{R_1 - R_2}{2} \tag{8}$$

Hence:

$$R_1 = R_{NOM} + \Delta R \tag{9}$$

If the resistors are now by some means transposed there are two possible output voltages for the circuit which we will refer to as Vo_a and Vo_b. For our circuit in its initial configuration we have:

$$Vo_a = R_1 Ic_1 - R_2 Ic_2$$

$$= 2\left(I\Delta R + \Delta I R_{NOM}\right) \tag{10}$$

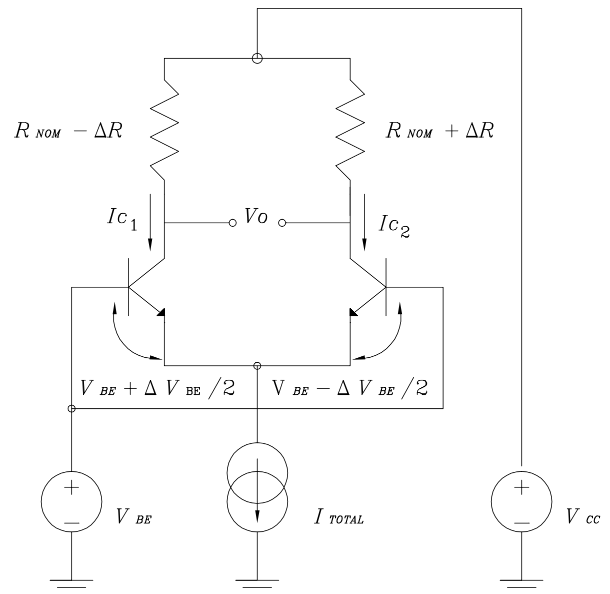


Fig (2) A Long Tailed Pair With Mis-matched Transistors and Resistors

Where *I* is the nominal collector current defined such that the currents flowing in each arm of the circuit are given by:-

$$Ic_1 = I + \Delta I \tag{11}$$

$$Ic_2 = I - \Delta I \tag{12}$$

After the resistors have been transposed we have:

$$Vo_b = 2\left(I\Delta R - \Delta I R_{NOM}\right) \tag{13}$$

Addition of (10) and (13) yields:

$$Vo_a + Vo_b = 4I\Delta R \tag{14}$$

Whilst subtraction of the same gives:

$$Vo_a - Vo_b = 4R_{NOM}\Delta I \tag{15}$$

Now

$$Vo = 2R_{NOM}\Delta I \tag{16}$$

so

$$Vo = \frac{(Vo_a - Vo_b)}{2} \tag{17}$$

If we now define the voltage across the ideal load resistor as V_{load} then:

$$V_{LOAD} = R_{NOM} I \tag{18}$$

Finally we substitute for (17) and (18) in (6) , which gives:

$$\Delta V_{BE} = \left(\frac{2\mathrm{kT}}{\mathrm{q}}\right) \operatorname{arctanh}\left(\frac{Vo_a - Vo_b}{4V_{LOAD}}\right) \tag{19}$$

If we now define resistor matching as the total difference in resistor values ($2\Delta R$) divided by R_{NOM}. Then from (14) and (18) we can calculate:

$$R_{MATCH}(\%) = 50\left(\frac{Vo_a - Vo_b}{V_{LOAD}}\right) \tag{20}$$

Where $R_{MATCH}(\%)$ is the percentage mis-match of the two resistors.

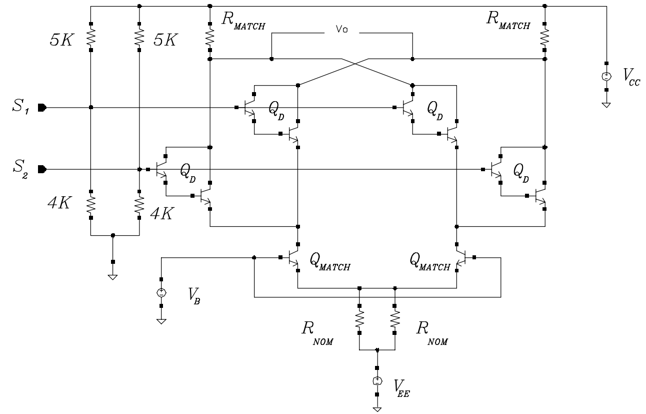
A PRACTICAL CIRCUIT

Fig(3) represents a practical circuit for component mis-match analysis. The load resistors are switched by means of four Darlington pairs to minimise the effect of switching component mis-match on the devices being matched. Switching is accomplished by grounding either node S_1 or S_2 to disable the requisite pair of Darlington switches.

The test sequence is as follows:

i) Ground S_1 float S_2

a) Measure V_{LOAD_a} (Voltage across L.H. R_{MATCH})
b) Measure Vo_a (Vo for this configuration)



Fig(3) A Differential Amplifier With Switchable Load Resistors

ii) Ground S_2 float S_1

a) Measure Vo_b (Vo for this configuration)

Thus by measuring only three voltages and noting that:

$$V_{LOAD} = V_{LOAD_a} + \frac{V_{oa}}{2} \tag{21}$$

we may by reference to (19) and (20) readily calculate both the resistor and transistor mis-match parameters. Error analysis and SPICE simulation [1] of Darlington switching mis-match shows that measurement resolution for ΔV_{BE} is better than +/- 30 µV and for R_{MATCH} (%) better than +/- 0.1%.

RESULTS

The circuit has been used to obtain matching data for transistors realised on both conventional bipolar technologies and more

novel structures [2][3][4]. Table(1). summarises transistor matching data obtained for a process that uses traditional photoengraving techniques to define the emitter window (Process WP). Figs(4), (5) and (6) show sample distributions for three of the transistor geometries featured in Tab(1) It should be noted that it is the standard deviation of the matching figure that is of importance. The mean value of any matching parameter should be zero given any arbitrary but consistent signing convention. The mean values are then merely indications of systematic bias and a function of any asymmetry in the circuit layout.

Transistor Geometry (Emitter Stripe)	Nominal Emitter Current	Mean	Sigma
1.5μm x 1.5μm	20 μ A	600 μ V	560 μ V
1.5μm x 1.5μm	200 μ A	650 μ V	590 μ V
1.0μm x 2.5μm	270 μ A	700 μ V	650 μ V
3.0μm x 3.0μm	940 μ A	200 μ V	400 μ V
3.0μm x 10.0μm	3.1 mA	180 μ V	260 μ V

Table(1) Typical V_{BE} Matching Results For a Photo-engraved (WP) Bipolar Technology

The G.E.C. Plessey 'HG' bipolar process is a modern high performance double poly-silicon process with spacer aligned emitter stripe and etched poly-silicon resistors. The as drawn emitter window has a minimum width of 0.6mm, which after the spacer deposition and etch results in a true electrical emitter width of only 0.3µm. It was thought that if as had been assumed, area offsets were foremost in producing transistor mis-match, then by far the greatest contribution would be from spacer deposition and etch. We would therefore expect all minimum width devices to exhibit similar matching statistics. We present resistor and V_{BE} mis-match data for three minimum width devices on 11 wafers of pre-production HG over 3 batches. Typically we have 60 sites per wafer giving a maximum of 660 observations per circuit. The data was collected by autoprobe and then filtered and analysed using the SAS software suite. Table(2) details the V_{BE} mis-match data and in Table(3) we show matching data for etched poly-silicon resistors of equal length with widths from minimum 0.6µm to 9.6 µm. Sample distributions are included in Fig(6) and Fig(7) for both resistor and V_{BE} matching.

Transistor Geometry (Emitter Stripe)	Nominal Emitter Current	Mean	Sigma
0.6μm x 3.0μm	150 μA	150 μ V	810 μ V
0.6μm x 5.4μm	320 μA	100 μ V	800 μ V
0.6μm x 10.2μm	1.28 mA	127 μ V	790 μ V

Table(2) Transistor Mis-match Data for Process HG Transistors

Resistor Geometry (W x L)	Resistor Type	Mean (%)	Sigma (%)
0.6μm x 100 μm (13.3 KΩ)	Low dose 'n' poly	−0.55	0.99
2.4μm x 100 μm (6.3 KΩ)	Low dose 'p' poly	−0.28	0.39
9.6μm x 100 μm (1.6 KΩ)	Low dose 'p' poly	0.03	0.17

Table(3) Resistor Mis-match Data for Process HG

Typically we see that for process WP the V_{BE} matching improves as the emitter area increases; this is consistent with our notion of mis-match being primarily associated with non-systematic photolithography errors. More recent work moreover [5] suggests that V_{BE} mis-match is insensitive to both device orientation and separation. For resistors, again we see a monotonic improvement in matching with resistor width. The rather 'flat' results for our minimum width process HG transistors would seem to confirm that the greatest process step variability is indeed seen at emitter side-wall definition and etch.

CONCLUSIONS

We have presented a circuit for rapid and direct extraction of both transistor and resistor mis-match data. The process has been extensively automated and used to gather data on both conventional and more novel bipolar technologies. The matching parameters extracted have measurement uncertainties of less than +/- 30 µV for V_{BE} mis-match and better than +/- 0.1 % for resistor mis-match. These data whilst primarily of interest to circuit designers can also be of use to the process engineer during the evaluation of critical novel process steps.

REFERENCES

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[2] S.D.Connor, "Component Matching on The FAB4 Test Drop-in.", G.P.S. internal engineering note. 4 January 1991.

[3] S.D.Connor, "Automated VBE and Resistor Matching Measurements on Process WP", G.P.S. internal engineering note No 761, 9 January 1992.

[4] S.D.Connor, "Component Mis-match Data for Processes WP and WQ", G.P.S. internal engineering note No 854, 20 June 1992.

[5] Private communication from I.M. Stubbs, Senior Engineer G.E.C. Plessey Semiconductors plc.

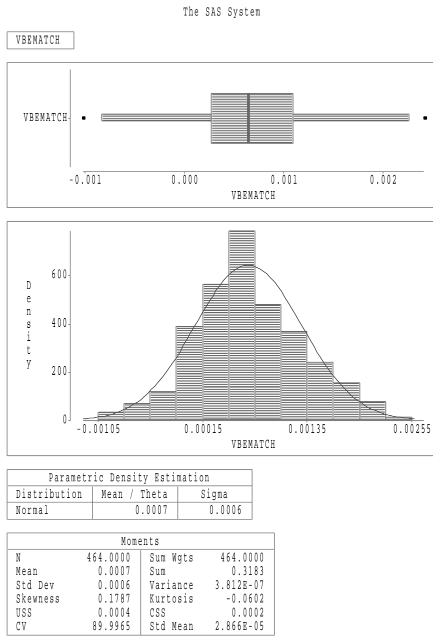


Fig (4) Sample Data Distribution For 'WP' 1.5μmx1.5μm Transistor Geometry V_{BE} Mis-match

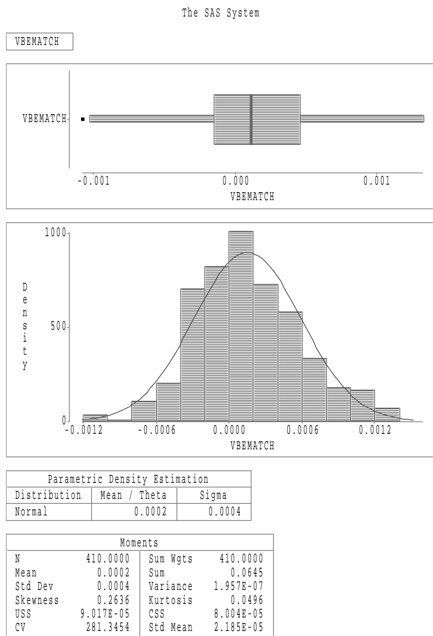


Fig (5) Sample Data Distribution For 'WP' 3.0μmx3.0μm Transistor Geometry V_{BE} Mis-match

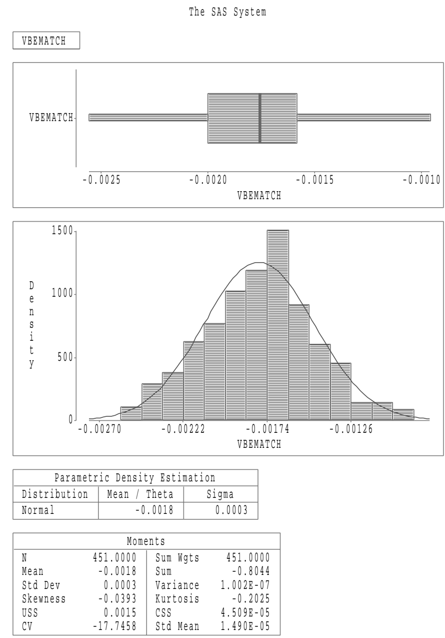
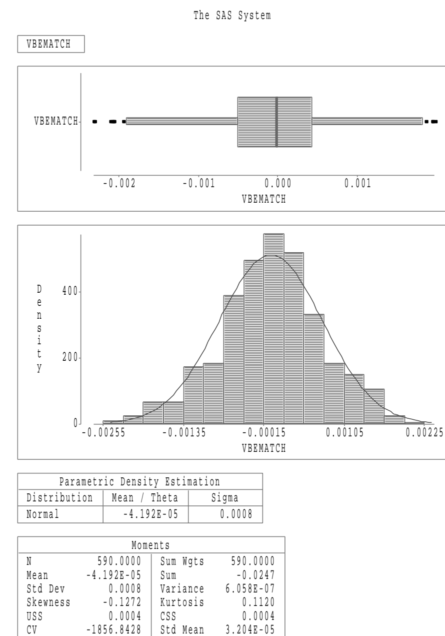


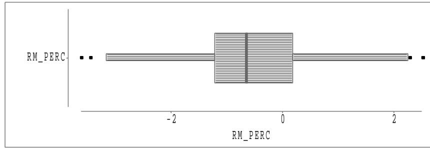
Fig (6) Sample Data Distribution For 'WP' 3.0μmx10.0μm Transistor Geometry V_{BE} Mis-match

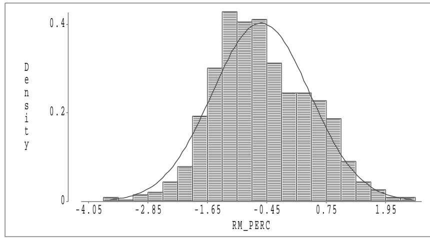


Fig(7) Sample Data Distribution for V_{BE} Mis-match using 0.6 by 3.0 μm Transistor

The SAS System

RM_PERC





Parametric Density Estimation		
Distribution	Mean / Theta	Sigma
Normal	-0.5460	0.9898

Moments			
N	584.0000	Sum Wgts	584.0000
Mean	-0.5460	Sum	-318.8637
Std Dev	0.9898	Variance	0.9798
Skewness	0.1950	Kurtosis	-0.0401
USS	745.3175	CSS	571.2181
CV	-181.2903	Std Mean	0.0410

Fig(8) Sample Data Distribution for Resistor Mis-match using 0.6 by 100 μm Resistor